IN THE SPECIFICATIONS

Please amend pgs. 11, 12, 14, 16, and 17 as follows:

Pg. 11

The chip 13 is formed by a semiconductor substrate such as silicon, and various elements such as a transistor not shown in the drawing are formed on the bottom main surface of the chip 13 and are covered with a protective dielectric film such as a passivation film. On the surface of the protective dielectric film or on the bottom surface of the chip are formed and arranged ball electrodes 31 made of solder, connected to the above elements, acting as internal electrodes. The ball electrodes 31 are soldered to the interconnect pads 21 formed on the packaging substrate 12 to mount the chip 13 on the packaging substrate 12 in a face-down manner, and the elements in the chip 13 are electrically connected to the ball electrodes 24 on the bottom surface of the packaging substrate 12 through intermediary of the ball electrodes 31 and the interconnect pads 21. The chip 13 is sealed is sealing resin 28.

In the first embodiment, the semiconductor device 11 is mounted on a dielectric substrate, mounting substrate 14. A specified interconnect pattern is formed on the dielectric substrate by using a conductive film to prepare the mounting substrate 14. The interconnect pattern includes interconnect pads 41 connected to the ball electrodes 24 of the semiconductor device 11 and interconnect lines, not shown in the drawings, for connecting the

interconnect pads 41 among one another on the mounting substrate 14 or the interconnect pad 41 with interconnect lines not shown in the drawings for connecting the interconnect pad 41 to an external circuit.

An example of configuration will be described, referring to Fig. 4, in which the ball electrodes 31 are formed and arranged on the bottom surface of the chip 13 of the semiconductor device 11 and interconnect pads 21 are formed and arranged on the top surface of the packaging substrate 12 corresponding to the ball electrodes 31.

The interconnect pads 21 formed on the top surface of the packaging substrate 12 shown in Fig.5 are disposed corresponding to the ball electrodes 31 on the bottom surface of the chip 13. The ball electrodes 31 on the bottom surface of the chip 13 are arranged in the shape of a lattice and the interconnect pads 21 are also arranged in the shape of the lattice corresponding to the ball electrodes 31. The specified number of the ball electrodes 31 and the interconnect pads 21 are grouped as a single I/O cell as shown in Fig.5 in which only the interconnect pads 21 are shown, and these are arranged as the I/O cell unit. In the embodiment, the plenty of the interconnect pads 21 are divided such that the single I/O cell includes an array of 4 x 3 interconnect pads 21. The

22a are connected to each of the interconnect pads 21a of the two outer peripheral I/O cells (CELL-A), and are drawn between the interconnect pads 21a to regions external to the chip 13. On the other hand, the interconnect lines 22b are connected to each of the interconnect pads 21b of the inner peripheral I/O cell (CELL-B), and are drawn similarly to the preceding example in the region of the peripheral I/O cell (CELL-B), and are bundled at a specified interval, at a region out of the inner peripheral I/O cell (CELL-B), to be drawn between the outer peripheral I/O cells (CELL-A) to regions external to the chip 13.

In the structure of the interconnect pads 21 and the interconnect lines 22 on the packaging substrate 12, the density of arranging the interconnect lines 21a at the I/O cells (CELL-A) arranged on the outer periphery of the chip 13 is substantially same as the density of the conventional device shown in Fig.3. However, the density of arranging the interconnect lines 22b connected to the interconnect pad 21b of the I/O cells (CELL-B) arranged inside of the chip 13 can be increased because of the absence of the interconnect pads.

Especially, as shown in Fig.6, since the interconnect lines of the other I/O cells do not pass through the I/O cells (CELL-B) disposed on the inner section of the chip, the I/O cells (CELL-B) may be formed to enable the arrangement of the extremely larger number of the ball electrodes 31 and the interconnect pads 21. An interval may exist between the I/O cells (CELL-B) disposed on the inner section. The ball electrodes 31 and the interconnect pads 21 of the outer peripheral I/O cells (CELL-A) may be freely disposed so long as the spaces through which the interconnect lines 22 of the I/O cells (CELL-B) disposed on the inner section pass may be secured, thereby promoting the higher integration of the semiconductor device having the higher performances. The I/O cells can be freely disposed in the regions of the chip so long as the above requisites are satisfied to increase the freedom of the chip design and the package design.

Since the interconnect pads 21 and the interconnect lines 22 in the embodiment are made by the conductive film having the single layer, the interconnect lines connected to the single I/O cell are not crossed in the vertical direction to easily perform the impedance matching on each of the interconnect lines.